



U.S. Department of Commerce, Patent and Trademark Office				Atty. Docket No.		Serial No.		
				DIN006-IC US		09/849,005		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicants: Chian-Min Ho et al.				
(Use several sheets if necessary)								
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				MAY 4, 2001		2123		
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
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	AB	5,630,051	5/13/97	Sun et al.	395	183.08		
	AC	5,600,787	2/4/97	Underwood et al.	395	183.06		
	AD	5,623,499	4/22/97	Ko et al.	371	22.1		
	AE	5,654,657	8/5/97	Pearce	327	163		
	AF	5,729,554	3/17/98	Weir et al.	371	27		
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							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
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	AI	Windley, Phillip J., "Formal Modeling and Verification of Microprocessors", IEEE Transactions on Computers, Vol. 44, No. 1, January 1995, pp. 54-72.						
	AJ	Clarke, E. M., et al., "Efficient Generation of Counterexamples and Witnesses in Symbolic Model Checking", 32 <sup>nd</sup> Design Automation Conference, June 12-16, 1995, pp. 427-432.						
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	AI	Bombana, M., et al., "Design-Flow and Synthesis for ASICs: a case study", 32 <sup>nd</sup> Design Automation Conference, June 12-16, 1995, pp. 292-297.					
	AJ	Beer, Ilan, et al., "Methodology and System for Practical Formal Verification of Reactive Hardware", 6 <sup>th</sup> International Conference, CAV '94, June 21-23, 1994, Proceedings, pp. 183-193.					
	AK	Daga, A., "A Symbolic-Simulation Approach to the Timing Verification of Interacting FSMs", International Conference on Computer Design: VLSI in Computers & Processors, October 2-4, 1995, 584-589.					
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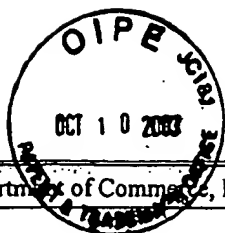
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PART "B"  
Sheet 8 of 24

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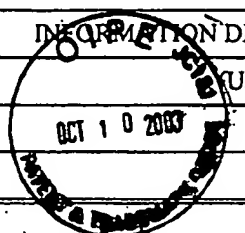
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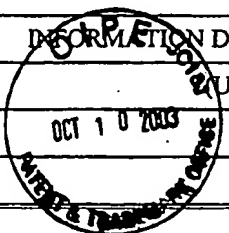
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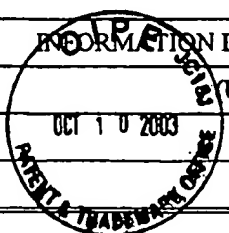
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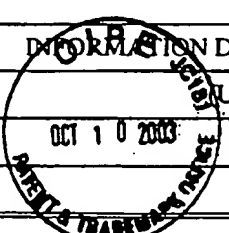
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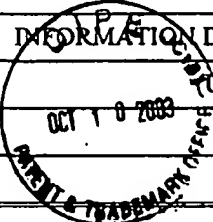
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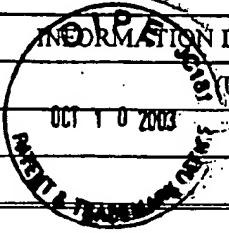


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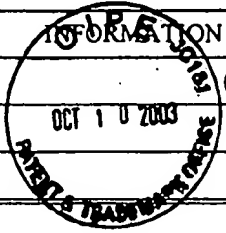
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PART "B"

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U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.	
				01N006-1CUS		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicants: Chian-Min Ho et al.			
(Use several sheets if necessary)							
				Filing Date		Group	
				MAY 4, 2001		2123	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AG						
	AH						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
	AI	Seawright, A., et al., "A System for Compiling and Debugging Structured Data Processing Controllers", EURO, Design Automation Conference, 1996.					
	AJ	Data Sheet "ATC's CoverMeter™ USA Commercial Price List, 1996.					
	AK	Dill, D. L., et al., "Acceptance of Formal Methods: Lessons From Hardware Design", Computer, April 1996, pp. 23-24.					
	AL	Bullis, D., "Verification and Modeling for Synthesis-Based Design", Marketing Communications, believed to be prior to 1997, pp. 15-17.					
	AM	Article "Product expectations in networking have risen to a point where systems must be self-correcting. The added cost of 'safe' design practices is not even questioned", Electronic Engineering Times, November 11, 1996, p. 48.					
	AN	Young, L. H., "Building A Better Bug Trap", Electronic Business Today, November 1996, pp. 49-53.					
	AO	Silbey, A. "The Systems Challenge for EDA Tools" Viewlogic Systems, believed to be prior to October 1997, pp. 22-26.					
Examiner				Date Considered			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							



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	AG						
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
	AI	Singer, S., et al., "Next Generation Test Generator (NGTG) for Digital Circuits", AUTOTESTCON, 97. 1997 IEEE Autotestcon Proceedings, Septe. 22-25, 1997, pp. 105-112.					
	AJ						
	AK						
	AL						
	AM						
	AN						
	AO						
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